

## WHAT IS CLAIMED IS:

- 1        1. An debug and emulation system comprising:
  - 2        a target device embodied in a single integrated circuit
  - 3        including
    - 4            an function clock circuit generating an function
    - 5            clock;
    - 6            an operation circuit connected to said function
    - 7            clock circuit operating in synchronism with said function
    - 8            clock;
    - 9            a trace trigger circuit connected to said function
    - 10          clock circuit and said operation circuit, said trace
    - 11          trigger circuit triggering trace of operation of said
    - 12          operation circuit upon detection of a predetermined
    - 13          condition within said operation circuit;
    - 14          a reference clock input for receiving a reference
    - 15          clock signal;
    - 16          a clock circuit connected to said function clock
    - 17          circuit for receiving said function clock signal and to
    - 18          said reference clock input for receiving said reference
    - 19          clock signal, said clock circuit generating an oscillator
    - 20          clock signal synchronous with one of said function clock
    - 21          circuit and said reference clock signal;
    - 22          a trace first-in-first-out buffer having an input
    - 23          connected to said function clock circuit and said
    - 24          operation circuit for storing trace data in synchronism
    - 25          with said function clock signal and an output connected
    - 26          to said phase locked loop clock circuit for outputting
    - 27          trace data in synchronism with said oscillator clock
    - 28          signal; and

29           a trace output port connected to said output of  
30       said trace first-in-first-out buffer outputting trace  
31       data from said target device; and  
32       an emulator connected to said trace output port for  
33       sensing said trace data in synchronism with said oscillator  
34       clock signal.

1       2. The debug and emulation system of claim 1, wherein:  
2       said emulator includes  
3           a reference clock generator connected to said  
4       reference clock input for generating said reference clock  
5       signal; and  
6           a clock control circuit connected to said clock  
7       circuit of said target device for controlling whether  
8       said oscillator clock signal is synchronous with said  
9       function clock circuit or with said reference clock  
10       signal.